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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,437	12/05/2003	James M. Cleeves	MA-110	9392

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,437	CLEEVES ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) *19-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the election filed October 28, 2005.

Election/Restrictions

2. Applicant's election with traverse of Embodiment I in the reply filed on 10/28/05 is acknowledged. The traversal is on the ground(s) that claim 1 is generic to claims 19, 24, 34 and 46. This is not found persuasive because claim 1 is not generic to claims 19, 24, 34 and 46. For example, in claim 1 it states "the first above device level having a first above-substrate pitch wherein the first above substrate pitch is smaller than the substrate pitch" and claim 46 states "the first above device level having a first above-substrate critical dimension wherein the first above substrate critical dimension is smaller than the substrate critical dimension." Therefore, the claims are not generic.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

3. Claim 16 is objected to because of the following informalities: a) it depends from itself. Appropriate correction is required.

Information Disclosure Statement

4. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Specification

5. The disclosure is objected to because of the following informalities: a) Applicant needs to provide the application number for the related application (See Paragraph 1).

Appropriate correction is required.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following must be shown or the feature(s) canceled from the claim(s): a) a substrate device level (See Claim 1); b) a first above substrate device level formed above the substrate device level (See Claim 1); c) the first above-substrate device level having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch (See Claim 1); d) the first above substrate device level comprises a first plurality of memory cells (See Claim 2); e) the first above substrate device level comprises a driver circuitry (See Claim 3); f) a first area, said area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch; g) a die includes dummy structures (See Claim 9); h) a second above substrate level formed over the first above substrate device level; i) memory array comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line (See Claim 13); j) the memory array comprises word lines segments and a word line driver circuit in the substrate (See Claim 13); and k) memory cells are arranged in series-connected NAND strings (See Claim 18). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (U.S. Patent No. 6,631,085) in view of Owada et al. (U.S. Patent No. 5,060,045).

In regards to claim 1, Kleveland et al. ("Kleveland") discloses the following:

a) a substrate device level (For Example: See Figure 12); and

b) a first above substrate device level formed above the substrate device level (For Example: See Figure 12).

In regards to claim 1, Kleveland fails to disclose the following:

a) the first above-substrate device level having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch.

However, Owada et al. ("Owada") discloses a first above-substrate device level having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include a first above-substrate device level having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch as disclosed in Owada because it aids in increasing the versatility of the wiring (For Example: See Column 4 Lines7-24).

Additionally, since Kleveland and Owada are both from the same field of endeavor, the purpose disclosed by Owada would have been recognized in the pertinent art of Kleveland.

In regards to claim 2, Kleveland discloses the following:

a) the first above substrate device level comprises a first plurality of memory cells (56 and 58) (For Example: See Abstract and Figure 12).

In regards to claim 3, Kleveland discloses the following:

a) the first above substrate device level comprises a driver circuitry (For Example: See Figure 12 and Column 8 Lines 64-66).

In regards to claim 12, Kleveland discloses the following:

a) the plurality of memory cells form part of a monolithic three dimensional memory array (For Example: See Figure 12).

In regards to claim 15, Kleveland discloses the following:

a) the memory cells are passive element memory cells (For Example: See Column 15 Lines 41-46).

In regards to claim 16, Kleveland discloses the following:

a) the memory cells are antifuse diode cells (For Example: See Column 4 Lines 24-36).

9. Claims 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (U.S. Patent No. 6,631,085) in view of Owada et al. (U.S. Patent No. 5,060,045) and Cleeves et al. (U.S. Patent No. 6,486,066).

In regards to claim 4, Kleveland fails to disclose the following:

a) a first area, said area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch.

However, Cleeves et al. ("Cleeves") discloses a first area (202) comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area (204) having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch (For Example: See Figure 2B). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include a first area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch as disclosed in Cleeves because it aids in providing uniform device density (For Example: See Column 6 Lines 24-28).

Additionally, since Kleveland and Cleeves are both from the same field of endeavor, the purpose disclosed by Cleeves would have been recognized in the pertinent art of Kleveland.

In regards to claim 5, Kleveland discloses the following:

a) the first area comprises a plurality of substantially parallel, substantially coplanar rails (For Example: See Figure 12).

In regards to claim 6, Kleveland fails to disclose the following:

a) photolithography processes are optimized to minimize the first above substrate pitch of the plurality of rails in the first area.

However, the following limitation makes it a product by process claim: a) "photolithography processes are optimized to minimize the first above substrate pitch of the plurality of rails in the first area." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 7, Kleveland fails to disclose the following:

a) the plurality of rails is patterned using off-axis illumination.

However, the following limitation makes it a product by process claim: a) "patterned using off-axis illumination." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 8, Kleveland fails to disclose the following:

a) the plurality of rails is patterned using a dipole illumination aperture.

However, the following limitation makes it a product by process claim: a) "patterned using a dipole illumination aperture." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based

upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 9, Kleveland fails to disclose the following:

a) a die includes dummy structures.

However, Cleeves discloses a die including dummy structures (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include a die including dummy structures as disclosed in Cleeves because it aids in enhancing chemical mechanical planarization (For Example: See Column 1 Lines 28-31).

Additionally, since Kleveland and Cleeves are both from the same field of endeavor, the purpose disclosed by Cleeves would have been recognized in the pertinent art of Kleveland.

In regards to claim 10, Kleveland fails to disclose the following:

a) a second above-substrate device level formed over the first above-substrate device level, the second above-substrate device level having a second above-substrate pitch, wherein the second above-substrate pitch is smaller than the substrate pitch.

However, Owada discloses a second above-substrate device level formed over the first above-substrate device level, the second above-substrate device level having a second above-substrate pitch, wherein the second above-substrate pitch is smaller than the substrate pitch (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include a second above-substrate device level formed over the first above-substrate device level, the second above-substrate device level having a second above-substrate pitch, wherein the second above-substrate pitch is smaller than the substrate pitch as disclosed in Owada because it aids in increasing the versatility of the wiring (For Example: See Column 4 Lines7-24).

Additionally, since Kleveland and Owada are both from the same field of endeavor, the purpose disclosed by Owada would have been recognized in the pertinent art of Kleveland.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (U.S. Patent No. 6,631,085) in view of Owada et al. (U.S. Patent No. 5,060,045) and Mitsubishi Electric (Japanese Publication No. 3393923).

In regards to claim 13, Kleveland fails to disclose the following:

a) memory array comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line.

However, Mitsubishi discloses a memory array that comprises segmented bit lines and global bit lines, wherein two segmented bit lines (SBL1 and SBL2) share a vertical connection to an associated global bit line (GBL1) (For Example: See Figure 1). It would have been obvious

to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include memory array that comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line as disclosed in Mitsubishi because it aids in reducing power consumption (For Example: See Abstract).

Additionally, since Kleveland and Mitsubishi are both from the same field of endeavor, the purpose disclosed by Mitsubishi would have been recognized in the pertinent art of Kleveland.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (U.S. Patent No. 6,631,085) in view of Owada et al. (U.S. Patent No. 5,060,045) and Pio (U.S. Publication No. 2003/0198101).

In regards to claim 14, Kleveland fails to disclose the following:

a) the memory array comprises word lines segments and a word line driver circuit in the substrate.

However, Pio discloses a memory array that comprises word lines segments and a word line driver circuit in the substrate (For Example: See Page 6-Claim 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include a memory array that comprises word lines segments and a word line driver circuit in the substrate as disclosed in Pio because it aids in preventing stored data from being erased (For Example: See Paragraph 15).

Additionally, since Kleveland and Pio are both from the same field of endeavor, the purpose disclosed by Pio would have been recognized in the pertinent art of Kleveland.

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (U.S. Patent No. 6,631,085) in view of Owada et al. (U.S. Patent No. 5,060,045) and Young (U.S. Patent No. 5,621,683).

In regards to claim 17, Kleveland fails to disclose the following:

a) the memory cells are thin film transistors having a charge-storage dielectric.

However, Young discloses memory cells that are thin film transistors having a charge-storage dielectric (For Example: See Column 4 Lines 35-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include memory cells that are thin film transistors having a charge-storage dielectric as disclosed in Young because it aids in reducing costs (For Example: See Column 3 Lines 34-38).

Additionally, since Kleveland and Young are both from the same field of endeavor, the purpose disclosed by Young would have been recognized in the pertinent art of Kleveland.

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland et al. (U.S. Patent No. 6,631,085) in view of Owada et al. (U.S. Patent No. 5,060,045), Young (U.S. Patent No. 5,621,683) and Nakai (U.S. Patent No. 5,587,948).

In regards to claim 18, Kleveland fails to disclose the following:

a) the memory cells are arranged in series-connected NAND strings.

However, Nakai discloses memory cells that are arranged in series-connected NAND strings (For Example: See Column 3 Lines 40-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of

Kleveland to include are arranged in series-connected NAND strings as disclosed in Nakai because it aids in extending the life of the chip (For Example: See Column 2 Lines 53-60).

Additionally, since Kleveland and Nakai are both from the same field of endeavor, the purpose disclosed by Nakai would have been recognized in the pertinent art of Kleveland.

Allowable Subject Matter

14. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

January 22, 2006